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CERTIFICATION

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of the German priority document bearing No. 198 43 624.6, filed with the German Patent Office on September 23, 1998.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Integrated circuit arrangement and method for its production

The invention relates to an integrated circuit arrangement which, in particular, can be implemented by using copper as conductive material.

New materials are increasingly being sought for future use in integrated circuit arrangements. Amongst others, copper is being investigated as conductive material.

In these new materials, one of the problems which arises is that semiconductor wafers, in particular silicon wafers, are contaminated by this material.

It has therefore been proposed (see, for example, M. Woo et al., 1998 Symp. VLSI Technology Digest of Technical Papers, pages 12 to 13, or L. Su et al., 1998 Symp. VLSI Technology Digest of Technical Papers, pages 18 to 19), in integrated circuits which contain copper as conductive material, to provide an insulating diffusion barrier between such conductive structures made of copper and the semiconductor substrate and, in the region of contacts of the conductive structure, to provide a conductive barrier to the semiconductor substrate. The intention of these barriers is to prevent diffusion of the contaminating conductive material from the conductive structure to the semiconductor substrate.

Furthermore, it has been proposed to provide diffusion barriers above such conductive copper structures, said barriers being preventing diffusion of copper into dielectric layers which are used as so-called intermetal dielectric between different metalization planes.

In order to produce an integrated circuit having two planes of conductive structures made of copper, it is known (see for example M. Woo et al., 1998 Symp. VLSI Technology Digest of Technical Papers, pages 12 to 13 or L. Su et al., 1998 Symp. VLSI Technology Digest of Technical Papers, pages 18 to 19) firstly to form the lower plane of conductive structures from copper. This lower plane is separated from the semiconductor substrate by diffusion barrier layers, conductive diffusion barriers being used in the region of contacts. An insulating diffusion barrier layer is applied to the entire area of the lower metalization plane, and a further dielectric layer, in which contact holes to the conductive structures of the lower metalization plane are opened, is applied to said insulating diffusion barrier layer. Then, firstly an electrically conductive barrier is applied and then the contact holes are filled with copper.

It has been shown that, even in this structure, contamination of the dielectric layer by copper occurs.

The invention is therefore based on the problem of specifying an integrated circuit arrangement which has at least two conductive structures and in which diffusion of the material from the conductive structures into the surrounding material is avoided. In addition, a method of producing such an integrated circuit arrangement is to be specified.

According to the invention, the problem is solved by an integrated circuit arrangement as claimed in claim 1, and a method for its production as claimed in claim 6. Further refinements of the invention emerge from the remaining claims.

Provided in the circuit arrangement according to the invention is a first conductive structure, which is embedded in a first

insulating layer. Above the first conductive structure there are arranged a diffusion barrier layer and a second insulating layer, in which a contact hole is provided which reaches as far as the first conductive structure. Above the diffusion barrier layer, the side walls of the contact hole are provided with spacers which act as barriers to diffusion of the material from the first conductive structure into the second insulating layer and which reach as far as the surface of the diffusion barrier layer. A second conductive structure, which is conductively connected to the first conductive structure, is arranged in the contact hole.

In order to produce an integrated circuit arrangement of this type, the diffusion barrier layer is applied to a substrate which has at least the first insulating layer with the first conductive structure. The second insulating layer is applied to said diffusion barrier layer. The contact hole is etched in the second insulating layer, above the first conductive structure, in which hole the surface of the first conductive structure is covered with the diffusion barrier layer. Then, on the side walls of the contact hole, the spacers are formed, which act as barriers to diffusion of the material from the first conductive structure into the second insulating layer. Then, the contact hole is opened as far as the surface of the first conductive structure and provided with the second conductive structure.

Since the side walls of the contact hole are covered with the spacers, which have a diffusion barrier effect, before the surface of the first conductive structure is exposed in the contact hole, in this circuit arrangement the situation is avoided where, when the contact hole is opened, material removed at the surface of the first conductive structure during the opening of the contact hole is deposited onto the

side walls of the second insulating layer. Depositions of this type during the etching of the contact hole are considered to be responsible for the fact that, in the circuit arrangements produced in accordance with known methods, in spite of the use of diffusion barriers, contamination of the dielectric layers occurs. In the method according to the invention, such deposition can take place only at the surface of the spacers or of the diffusion barrier layer. Since the spacers and the diffusion barrier layer constitute a diffusion barrier, contamination of the second insulating layer is effectively prevented.

The spacers are preferably formed from electrically conductive material with a diffusion barrier effect, since in this case, the effective conduction cross section of the second conductive structure is enlarged by the spacer cross-sectional area.

In order to avoid short circuits between the first conductive structure and adjacent conductive structures, it is advantageous to provide the diffusion barrier layer from an insulating diffusion barrier material, in particular SiN or SiON.

The circuit arrangement according to the invention, and the method for its production, can advantageously be applied when using materials for the first conductive structure and/or the second conductive structure which exhibit high diffusion into adjacent material. In particular, the circuit arrangement and the method for its production can advantageously be applied when using copper, silver, gold, platinum or palladium for the first conductive structure and/or the second conductive structure.

All materials with a diffusion barrier effect are suitable for the spacers, in particular SiN, SiON, Ta, TaN or Ti or TiN, conductive materials being preferred with regard to the conduction cross section.

The first conductive structure preferably adjoins a first diffusion barrier structure which is electrically conductive and which is arranged at least beneath and to the side of the first conductive structure and which acts as a barrier to diffusion of the material from the first conductive structure into adjacent material. In particular, Ta, TaN, Ti or TiN are suitable for the first diffusion barrier structure.

Moreover, it is advantageous, beneath the second conductive structure, to provide a second diffusion barrier structure which is electrically conductive and which adjoins the second conductive structure underneath and acts as a barrier to diffusion of the material from the second conductive structure. In particular, Ta, TaN, Ti or TiN are also suitable for the second diffusion barrier structure.

In the following text, the invention will be explained in more detail using an exemplary embodiment which is illustrated in the figures.

Fig. 1 shows a section through a substrate having a first insulating layer, in which a first conductive structure is embedded, having a diffusion barrier layer, which covers the first conductive structure, and having a second insulating layer, in which a contact hole is opened as far as the surface of the diffusion barrier layer.

Fig. 2 shows the section through the substrate after the deposition of a conformal barrier layer.

Fig. 3 shows the section through the semiconductor substrate after the formation of spacers with a diffusion barrier effect on the side walls of the contact hole.

Fig. 4 shows the section through the semiconductor substrate after exposure of the surface of the first conductive structure within the contact hole.

Fig. 5 shows the section through the semiconductor substrate after the formation of a second conductive structure.

A semiconductor substrate has at least one passivation layer 1 and an insulating diffusion barrier layer 2 arranged thereon. The semiconductor substrate consists of substantially monocrystalline silicon, the passivation layer 1 of SiO_2 and the insulating diffusion barrier layer 2 of SiN. Provided in the passivation layer 1 and the insulating diffusion barrier layer 2 is a terminal 3 made of polysilicon or tungsten, which is provided in order to make contact with a component implemented in the semiconductor substrate underneath the passivation layer 1 (see Figure 1).

Applied to the surface of the insulating barrier layer 2 are a first insulating layer 4 of SiO_2 or an organic or inorganic material with a lower dielectric constant than SiO_2, which is known to those skilled in the art as low k material, and for which polyamide or substances with the commercial designation PBO, BCB, Flowfill or Silk are suitable, in a layer thickness of 0.1 µm to 2 µm. Formed in the first insulating layer 4, by means of building an opening, depositing a first conductive barrier layer of Ta and depositing a copper layer, and also subsequent chemical mechanical polishing until the surface of the first insulating layer 4 is exposed, are a first diffusion

barrier structure 5 and a first conductive structure 6. The first diffusion barrier structure 5 adjoins the sides and the bottom of the first conductive structure 6. It prevents any diffusion of the copper from the first conductive structure 6 into the first insulating layer 4, and also into the terminal 3 located underneath and, via the latter, into the semiconductor substrate. The first conductive structure 6 is embedded in the first insulating layer 4.

Next, a first diffusion barrier layer 7 of SiN is applied in the lowest possible layer thickness of typically < 100 nm, preferably 10 to 50 nm. Applied to the diffusion barrier layer 7 is a second insulating layer 8 of SiO_2 or a low k material in a layer thickness of 0.1 µm to 2 µm. With the aid of an etching mask 9, a contact hole 10 is opened in a plasma etching process, said hole being arranged above the first conductive structure 6 and reaching as far as the surface of the diffusion barrier layer 7.

If the second insulating layer 8 consists of SiO_2, the etching mask 9 is formed of photoresist, polyimide or photoimide, and the plasma etching process is carried out by using an etching gas containing CF_4, CHF_3 and/or C_4F_8.

If the second insulating layer 8 consists of low k material, the etching mask 9 is formed of SiO_2, SiN or SiON, and the plasma etching process is carried out with an etching gas containing O_2 with the addition of N_2, CF_4 or the like.

After the etching mask 9 has been removed, a conformal diffusion barrier layer 11 of Ta is deposited, in a layer thickness of 10 to 50 nm, by means of PVD (Physical Vapor deposition) or CVD (Chemical Vapor deposition) (see Figure 2).

By means of anisotropic etching with fluorine chemistry (CF_4, CHF_3, for example $CF_4 + O_2$), spacers 11' are formed from the conformal barrier layer 11 on the side walls of the contact hole 10. The spacers 11' consist of TaN and have a diffusion barrier effect against copper (see Figure 3). The spacers 11' reach as far as the surface of the first diffusion barrier layer 7.

By means of anisotropic etching with fluorine chemistry, the diffusion barrier layer 7 is structured, so that the contact hole 10 reaches as far as the surface of the first conductive structure 6. During this etching step, that surface of the second insulating layer 8 that faces the contact hole is covered with the spacers 11', so that any deposition of material removed at the surface of the first conductive structure 6 onto the flanks of the second insulating layer 8 which face the contact hole 10 is avoided (see Figure 4). Alternatively, the etching of the spacers 11' and the structuring of the diffusion barrier layer 7 can be carried out in one etching step.

Then, a second conductive diffusion barrier layer is deposited, which covers the surface of the second insulating layer 8, the spacers 11' and the exposed surface of the first conductive structure 6. The second conductive diffusion barrier layer is formed of TaN, in a layer thickness of 10 nm to 50 nm, by means of PVD or CVD deposition. By depositing a further copper layer, which fills up the remaining clearance in the contact hole 10, and structuring the copper layer and the second conductive diffusion barrier layer arranged underneath it, a second diffusion barrier layer 12 and a second conductive structure 13 are formed, the latter being conductively connected to the first conductive structure 6 (see Figure 5). The second conductive structure 13 is

configured as a conductor track belonging to a metalization plane.

Claims:

1. An integrated circuit arrangement,

- in which a first conductive structure (6) is provided, which is embedded in an insulating layer (4),

- in which, above the first conductive structure (6) there are arranged a diffusion barrier layer (7) and a second insulating layer (8), in which a contact hole (10) is provided which reaches as far as the first conductive structure (6),

- in which, above the diffusion barrier layer (7), the side walls of the contact hole (10) are provided with spacers (11'), which act as a barrier to a diffusion of the material from the first conductive structure into the second insulating layer (8) and which reach as far as the surface of the diffusion barrier layer (7),

- in which, in the contact hole (10) a second conductive structure is arranged, which is conductively connected with the first conductive structure (6).

2. The circuit arrangement as claimed in claim 1, in which the spacers (11') are electrically conductive.

3. The circuit arrangement as claimed in claim 1 or 2, in which the first conductive structure (6) adjoins a first diffusion barrier structure (5), which is electrically conductive and which is arranged at least beneath and to the side of the first conductive structure (6) and which acts as a barrier to diffusion of the material from the first conductive structure (6).

4. The circuit arrangement as claimed in one of claims 1 to 3, in which the second conductive structure (13) adjoins a second diffusion barrier structure (12), which is electrically conductive and is arranged at least beneath the second conductive structure (13) and which acts as a barrier to diffusion of the material from the second conductive structure (13).

5. The circuit arrangement as claimed in one of claims 1 to 4,

- in which the first conductive structure (6) and/or the second conductive structure (13) contains copper, silver, gold, platinum or palladium,

- in which the spacers (11') and/or the first diffusion barrier structure (5) and/or the second diffusion barrier structure (12) contain Ta, TaN, Ti or TiN,

- in which the diffusion barrier layer (7) and/or the spacers (11') contain SiN or SiON.

6. A method of producing an integrated circuit arrangement,

- in which a diffusion barrier layer (7) is applied to a substrate (1, 2, 3) which has at least a first insulating layer (4) in which a first conductive structure (6) is embedded,

- in which a second insulating layer (8) is applied to the diffusion barrier layer (7),

- in which a contact hole (10) is etched into the second insulating layer (8) above the first conductive structure (6),

in which hole the surface of the first conductive structure (6) is covered with the diffusion barrier layer (7),

- in which, on the side walls of the contact hole (10), spacers (11') are formed which act as a barrier to diffusion of the material from the first conductive structure (6) into the second insulating layer (8),

- in which the contact hole (10) is opened as far as the surface of the first conductive structure (6),

- in which, in the contact hole (10), a second conductive structure (13) is formed, which is conductively connected to the first conductive structure (6).

7. The method as claimed in claim 6, in which the spacers (11') are formed of electrically conductive material.

8. The method as claimed in claim 6 or 7,

- in which, in order to produce the first electrically conductive structure (6), the first insulating layer (5) is applied to the substrate (1, 2, 3),

- in which an opening is produced in the first insulating layer (4),

- in which, by depositing and structuring a first conductive barrier layer, a first diffusion barrier structure (5) is formed which is electrically conductive and which covers the bottom and the side walls of the opening,

- in which the first conductive structure (8) is formed by filling the opening with conductive material.

9. The method as claimed in one of claims 6 to 8,

- in which, after the contact hole (10) has been opened as far as the surface of the first conductive structure (6), a second conductive barrier layer is deposited,

- in which a conductive layer is deposited,

- in which, by structuring the conductive layer and the second conductive barrier layer, the second conductive structure (13) and a second diffusion barrier structure (12) arranged underneath the latter are formed.

10. The method as claimed in one of claims 6 to 9,

- in which the first conductive structure (6) and/or the second conductive structure (13) contain copper, silver, gold, platinum or palladium,

- in which the spacers (11') and/or the first diffusion barrier structure (5) and/or the second diffusion barrier structure (12) contain Ta, TaN, Ti or TiN,

- in which the diffusion barrier layer (7) and/or the spacers (11') contain SiN or SiON.

Abstract

Integrated circuit arrangement and method for its production

In an integrated circuit arrangement, above a first conductive structure (6) which is embedded in a first insulating layer (4) there are arranged a first barrier layer (7) and a second insulating layer (8), in which a contact hole (10) is provided which reaches as far as the first conductive structure (6). Above the first barrier layer (7), the side walls of the contact hole (10) are provided with spacers which act as a diffusion barrier and which reach as far as the surface of the first barrier layer (7). Arranged in the contact hole (10) is a second conductive structure (13), which is conductively connected to the first conductive structure (6). During the production of the contact hole, the spacers prevent deposition of material from the first conductive structure (6) on the surface of the second insulating layer (8).

Fig. 5